CLAIMS

1. A method of detecting a resistive path or a predetermined potential in electronic non-volatile memory devices that comprise at least one array or matrix of memory cells arranged in sectors organized in rows and columns, said sectors being adapted to be erased independently from each other by an erase algorithm, and said memory array being associated with at least one row-decoding circuit portion per sector, each said portion being supplied positive and negative voltages, characterized by:

forcing a read condition onto any incompletely erased sector;

scanning the rows of said sector to check the possible presence of a spurious current;

finding a row where said spurious current flows and electrically isolating it by re-addressing said row to a redundant row provided in the same sector.

2. A method according to claim 1, characterized in that said reading condition is forced whenever the issue of the erase algorithm is incomplete or negative.

3. A method according to claim 1, characterized in that the rows of a given sector are scanned, also checking the possible presence of said spurious discharge current in a conduction path leading to a positive power supply.

4. A method according to claim 1, characterized in that at least one switch is provided between each one of the decode blocks and respective positive and negative power supplies in order to isolate the failed row.

5. A method according to claim 1, characterized in that said re-addressing is effected by means of a redundance decode block incorporated inside the row-decoding circuitry.

6. A method according to claim 4, characterized in that said switches are driven by a logic operatively interlinked to the contents of redundance registers.

7. A method according to claim 3, characterized in that said spurious current is detected by comparison of a row node with a redundance node.

8. A method according to claim 7, characterized in that said comparison is performed by a compare block, that is input a reference signal produced from a redundant row and a row signal taken at the beginning of a row being scanned.

9. A method according to claim 1, characterized in the erase algorithm is re-started after the failed row is identified and electrically isolated.

10. A method according to claim 1, characterized in that the presence of said spurious current indicates at least one memory cell in an erase-fail state.

11. An integrated non-volatile memory device of the programmable and electrically erasable type, comprising a sectored array of memory cells arranged in rows and columns, with at least one row decode circuit portion per sector being supplied positive and negative voltages, characterized in that it comprises a redundant-row block within each sector and a compare block being input a reference signal from a redundant row and a row signal taken at one end of a row of the array being read.

12. A device according to claim 11, characterized in that it comprises:

a plurality of row decode blocks and at least one redundance decode block within the decoding circuitry;

between each one of the decode blocks and the respective positive and negative supplies, at least one switch for, in the course of erase, read or program

operations, isolating and relating to a redundant one even a single block having at least one row with a failed cell.

13. A device according to claim 11, characterized in that said switches comprise MOS transistors.

14. A device according to claim 11, characterized in that it includes a control logic for controlling said switches.

15. A device according to claim 14, characterized in that the operation of said logic is interlinked to the contents of redundance registers.